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Opportunities presented by advanced off-the-shelf signal processing technology

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Abstract. The UK Met Office is currently running a network of 12 radars (between 10 and 25 years old), producing rainfall rate products every 5 min. Five of those radars have Doppler capabilities, and up to 4 more Doppler radars are due to be added to the existing network within the next 2 years. The main mechanical components (radar antenna and pedestal) are in good condition and have an estimated remaining lifetime of at least 10 years.

Within this next decade, it is anticipated that high resolution, cloud resolving, NWP models will become operational and take over the short period forecasting functionalities. A feature of these models is likely to be the direct assimilation of multi-level radar data (both reflectivity and radial winds). To support NWP development, whilst avoiding premature replacement of the radar hardware, a programme of in-house development of the signal and data processing system was initiated. A key feature of this development is the use of Commercial Off The Shelf (COTS) hardware to enable the direct digitisation of the raw IF signal, therefore removing the need for complex analogue processors within the hardware of the radar-to-PC interface. The hardware cost of this upgrade is kept to a minimum (around £10 k per radar), by taking full advantage of general purpose technology that has the capability to host numerous functions previously carried-out on the analogue signal. This upgrade offers to maximise the benefits derived from existing assets, provide data for NWP, and centralise all fault and performance monitoring systems. This paper presents the design of the new receiver and digital signal processing system, along with preliminary results of radial wind measurements.

1 Introduction

The Met Office currently runs a network of 12 radars (between 10 and 25 years old), producing rainfall rate products every 5 min. Five of those radars have Doppler capabilities, and up to 4 more Doppler radars are due to be added to the existing network within the next 2 years. The main mechanical components (radar antenna and pedestal) are in good condition and have an estimated remaining lifetime of at least 10 years.

All of these radar sites are currently controlled by a in-house developed PC based processing system called Cyclops. This system does not have Doppler capability and it digitises the radar's Log Z output (i.e. the original radar analogue receiver is retained).

Running a network of mature radars means that there is a continual battle to deal with obsolescence at the component and sub-system level. At the same time, there is pressure to minimise running costs and if possible generate new radar capability/performance. To this end a new version of Cyclops is being developed, called Cyclops-D. This system digitises the radar data at the IF stage and can make Doppler measurements.

Cyclops-D will be introduced alongside a re-designed radar receiver in which a number of existing analogue receiver modules have been eliminated. This has been achieved whilst maintaining backward compatibility with the current radar hardware and operational version of the Cyclops system.

These two developments are described in more detail in Sect. 2, and some initial test results are shown in Sect. 3. The benefits of the new system are summarised in Sect. 4.

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2 Implementation Description

2.1 PC and Data Acquisition Board

The new processing system is entirely built using Commercial Off The Shelf (COTS) hardware. This has the advantage of greatly reducing the hardware cost of the system. Software development costs are high, but this strategy is cost effective because of the number of radars within the UK radar network.

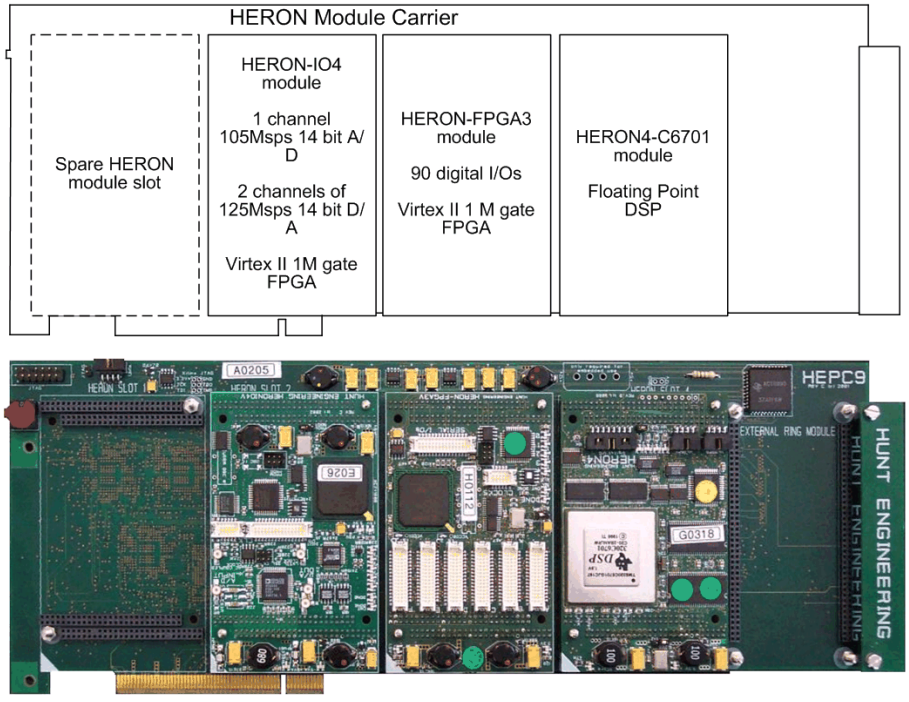

Fig. 1. Data Acquisition Board – Layout and Appearance.

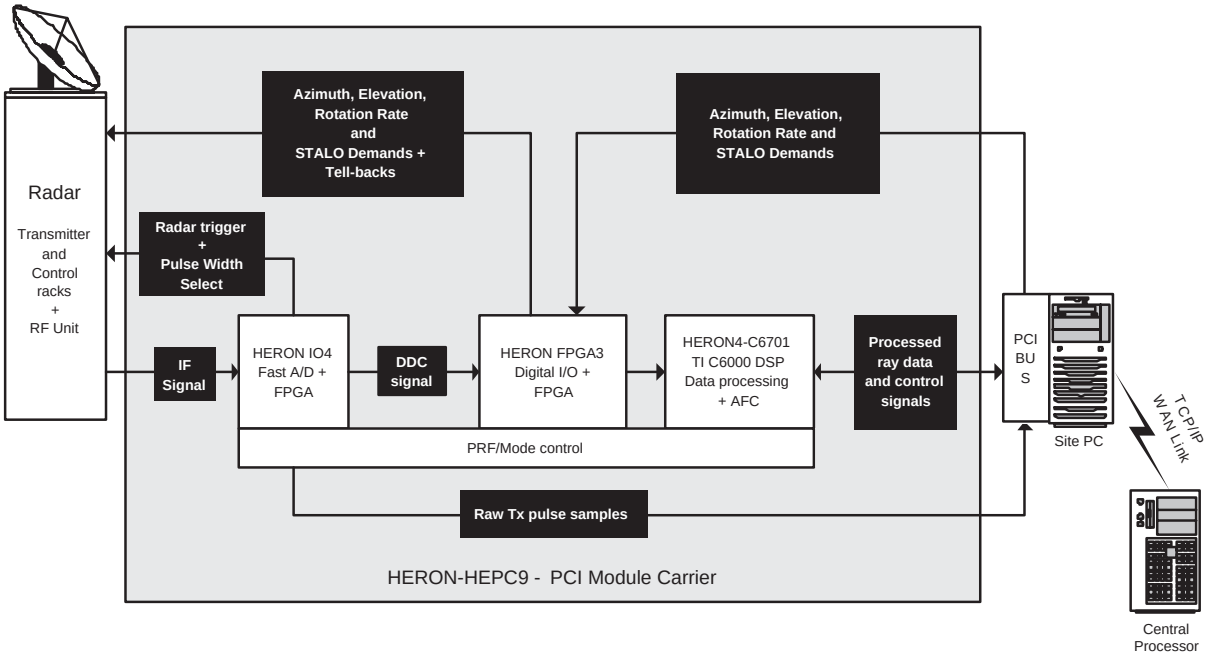

Fig. 2. Schematic Overview of the Cyclops D System Architecture.

The Cyclops-D system is built from a standard PC running Windows XP Professional. It is fitted with a PCI card manufactured by Hunt Engineering[1]. This card is the heart of the system and is made up of a Module Carrier board to which up to four plug-in modules can be fitted. A wide variety of I/O and processing modules are available. In the Cyclops-D configuration three modules are used (the fourth module position being left vacant). These comprise:

[1]Hunt Engineering Ltd, Brent Knoll, Somerset, UK. http://www.hunteng.co.uk

a) HERON Module Carrier board.

This provides real-time software configurable communication links between each of the modules and is capable of data rates up to 400Mbytes/second

b) HERON-IO4, with 1 channel of 105 Msps 14 bit A/D, 2 channels of 125 Msps 14 bit D/A and a Virtex II 1 M gate FPGA module.

The module is controlled by the FPGA (Xilinx Vertex–II). In addition to this the FPGA also controls 8 lines of user configurable digital I/O. The module is run at 100 MHz with sampling occurring at this rate. The duties of the FPGA on this module are: to carry out digital down conversion of the sampled IF, to provide non down-converted samples of the transmitted pulse for Automatic Frequency Control (AFC) purposes and to send trigger signals to the radar at the current PRF. In keeping with the COTS/low cost/rapid development theme the Digital Down-Conversion (DDC) (Andraka) (Hollis and Weir, 2003) is done using a readily available DDC core from Xilinx (Xilinx, 2002), which simply takes the parameters of the sampled signal, decimation rates, compensating and programmable FIR filter coefficients and generates a unit that can be used in your FGPA. The output of the DDC unit is a 2 MHz stream of complex baseband samples. These are passed by the module carrier to the digital I/O module.

c) HERON-FPGA3, with 90 digital I/Os and a Virtex II 1 M gate FPGA. module.

These I/O lines are used for antenna demands and tell-back data and also for demands to digital STable Local Oscillator (STALO) unit. The unit tags the complex baseband samples for each pulse with the current azimuth and elevation, and then passes them on to the DSP module.

d) HERON4-C6701 floating point DSP module.

The DSP is a Texas Instruments C6701 floating point processor capable of a peak processing speed of 1 GFlops. The main purpose of the DSP it to provide a real-time processing system which can then pass averaged data up to the PC for product generation and transmission. This includes recohering of data, pulse pair processing and time averaging.

Figure 1 shows the board layout and appearance.

The PC receives, via the PCI bus, completed rays from the DSP. It then carries out range averaging, calibration and if in dual PRF mode, velocity unfolding. Once the rays are completed they are packaged into a Met Office polar data format and transmitted by over a dedicated TCP/IP network for further processing at the Met Office headquarters in Exeter.

The PC is also responsible for reception of raw samples of the transmitted pulse, from which it calculates the current transmitter frequency and can adjust the STALO frequency via the digital I/O module.

Figure 2 shows a schematic overview of the system architecture

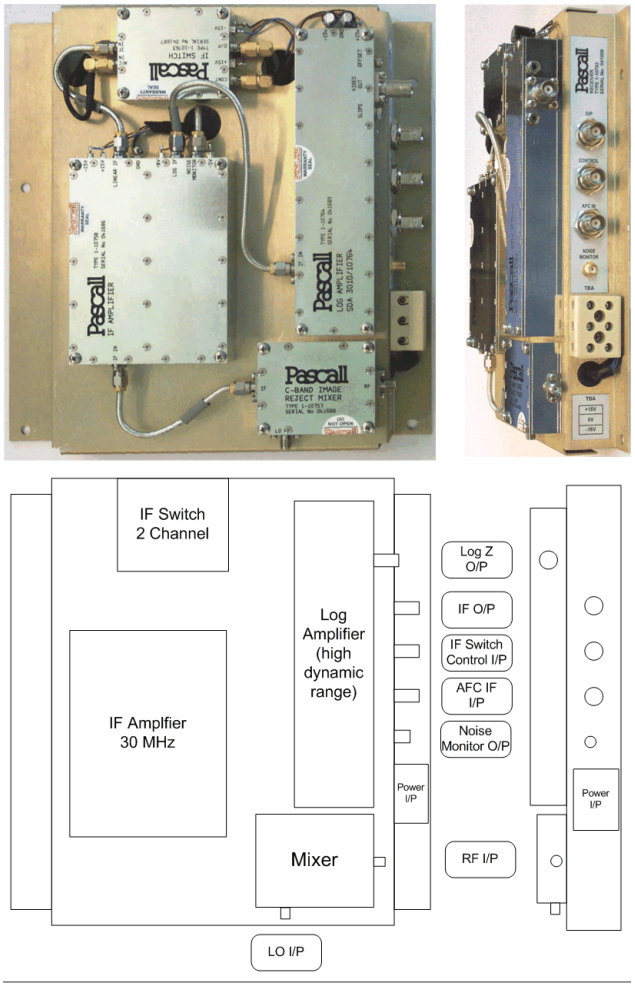

Fig. 3. Receiver Chassis – Layout and Appearance.

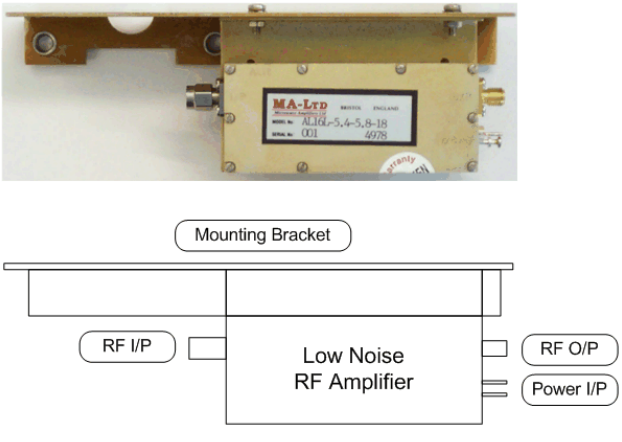

Fig. 4. Receiver Low Noise RF Amplifier – Layout and Appearance.

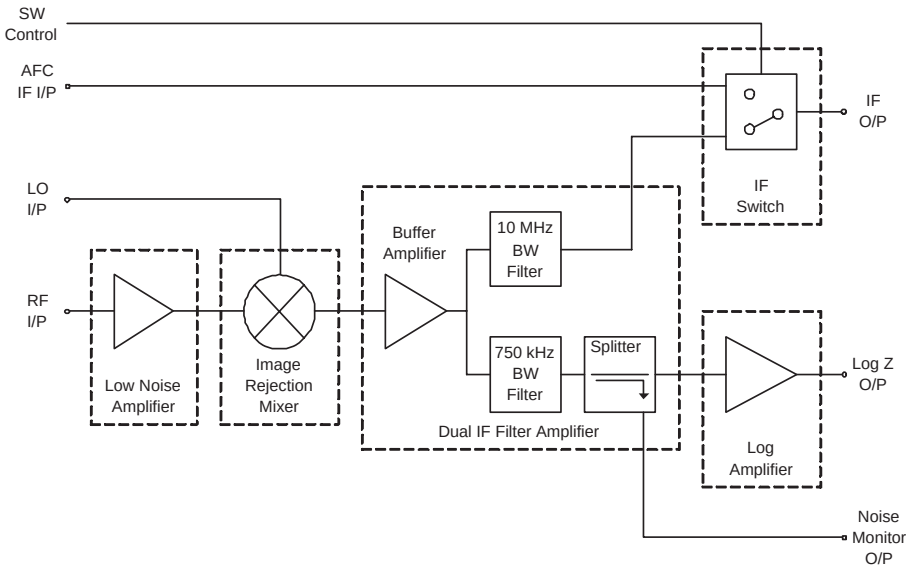

Fig. 5. Receiver – Functional Schematic.

2.2 Receiver

The existing analogue receivers were designed by Pascall Electronics[2] in 1983. The re-design (also by Pascall) exploits the technological advantages that have been made since and incorporates features that are necessary for the Cyclops-D implementation whilst maintaining compatibility with the existing radar hardware and Cyclops processor.

The receiver has three signal paths:

a) from RF I/P to Log Z output, this path maintains compatibility with the current processor. It has been designed with an increased dynamic range so that swept gain is not required. Another area which has received particular attention is the thermal stability, as the current design has a tendency to drift at high power levels.

b) from the RF I/P to the Noise Monitor O/P, this path maintains compatibility with the radar monitoring equipment.

c) from the RF I/P and AFC IF I/P to the IF O/P, this is the path used into Cyclops D. The Signal IF and the AFC IF are fed to Cyclops D via a high speed electronic switch (Watson et al., 2003). A switch is needed because there is only one channel of A/D conversion available.

It is used in this way:

a) When the transmitter is fired, the switch routes an IF sample of the transmitter's pulse to the A/D. This pulse contains the information needed to extract coherent data and hence Doppler information from the signal returns.

b) A few microseconds after the transmitter pulse, the switch routes the IF signal returns to Cyclops D.

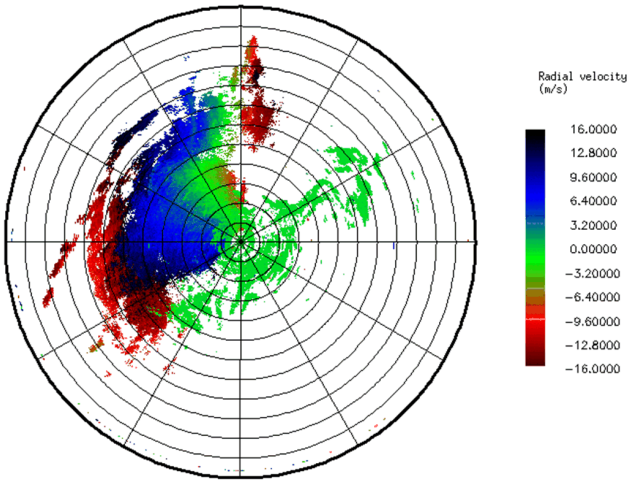

Fig. 6. First Doppler winds from Cyclops D test at Cobbacombe Cross (18th March 2004. Maximum range 120 km, p.r.f 1200 pps).

Through the use of an IF switch, only a single high speed A/D is needed, which reduces the overall the cost of the system.

Figure 3 shows the receiver's chassis layout and appearance.

Figure 4 shows the receiver's Low Noise RF Amplifier's layout and appearance.

Figure 5 shows a functional schematic of the receiver.

[2]Pascall Electronics Ltd, Cowes, Isle-of-Wight, UK. http://www.pascall.co.uk

3 Initial Results

An initial trail of some Cyclops-D functionality was carried out – mainly to test the signal processing within the FPGAs. The new system was connected to the operation weather radar at Cobbacombe Cross. It successfully controlled the radar antenna and transmitter and collected a limited amount of raw sample I and Q data. Data was collected with the radar running in:

a) Long Pulse (2 microsecond pulse) at a p.r.f. of 300 Hz, processed to a range of 250 km.

b) Short Pulse (0.5 microsecond pulse) at a p.r.f. of 900 Hz and 1200 Hz in single and dual p.r.f. modes, processed to a range of 120 km.

The raw data was then processed offline and analysed to produce the Doppler winds and Reflectivity products.

This test did serve to highlight a problem with an excessive amount of noise being introduced at the analogue to digital stage. This severely reduced the signal to noise ratio and hence the dynamic range of the system. On investigation it was found that the majority of this noise was being introduced by the close proximity of the PCs AGP graphics card to the module carrier. Removing this AGP card and using the PC's built-in graphics has reduced the noise levels in the converter to more manageable levels.

Some preliminary radial wind data from Cyclops-D are shown in Fig. 6. A high noise threshold was applied to the data to reduce the impact of the noise problem noted above. These data do not suggest any problems so far in the accuracy of the phase detection, at least at moderate and high signal levels.

4 Summary of Benefits

– Availability of off-the-shelf general purpose PC-based systems has dramatically cut the cost of radar signal and data processing. The investment in software development is relatively high, but is cost-effective for a network composed of a large number of identical radars.

– The new receiver design allows for smooth migration between the existing and new systems, minimising risks and radar downtime.

– Processing of digitized IF enables IF power and transmitter frequency to be accurately monitored, eliminating the need for the existing radar subsystems which currently carry out these functions.

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